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09/842,435	04/25/2001	Brian William Hughes	10004546-1	7471

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,435	HUGHES ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-29* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 18-20 have been considered but are moot in view of the new ground(s) of rejection.

The Applicant contends, "The Examiner does not dispute that Eaton discloses a memory system that is operable to logically remap defective memory locations to replacement memory locations using substitute memory table 3-1 1. (column 5, lines 16-19) The substitute memory table of Eaton can either be a look-up table for all memory locations, or a content addressable memory to look up only replaced memory locations. (column 5, lines 20-40 and column 7, lines 21-28) In either case, Eaton's only disclosed means of replacing defective memory locations requires a mapping function in some type of memory, meaning that Eaton logically remaps defective memory cells, in contrast to the physical re-mapping of claim 18".

The Examiner disagrees and asserts that nowhere in the Eaton patent does Eaton ever mention logical remapping. Logical remapping is purely a fabrication of the Applicant's active imagination. Col. 7, lines 5-15 in Eaton teach that ECC Engine 3-3 of Figure 3 in Eaton is used to identify hard and soft errors at a memory location or cell. A memory cell is a physical element on a semiconductor chip for storing data. One of ordinary skill in the art at the time the invention was made would have known hard errors are errors at a memory cell on a semiconductor chip at a physical location on the semiconductor

chip. Col. 7, lines 21-24 in Eaton teaches that the group of declared defective memory cells are taken out of use and replaced or remapped to replacement memory cells 3-5c in Figure 3. The replacement memory cells are also physical elements having a physical location on a semiconductor chip. If a memory cell at a physical location on a semiconductor chip is found to be faulty, the faulty memory cell is remapped to a replacement memory cell at a physical location on the semiconductor chip that is presumed not to be defective. Figure 3 in Eaton explicitly depicts representations of physical memory cells. It would be nonsensical to allow the use of a known physically defective memory cell at a known physical site. The only thing that Eaton does not do is use the same language as the Applicant and it appears the Applicant is attempting to gain a patent on pure semantics and word games. However to accommodate the Applicant, the Examiner provides a new grounds of rejection whereby the same language that the Applicant uses is used in the Prior Arts for the grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) in view of Harns; Timothy (US 4460997 A) in further view of Morley; Richard E. (US 4506362 A).

35 U.S.C. 103(a) rejection of claim 18.

Eaton teaches evaluating elements of a memory segment (col. 4, lines 41-47 in Eaton teach that Figure 3 of Eaton is comprises of IC chips 3-1; Note: an IC chips 3-1 in Figure 3 is a memory segment); identifying faulty ones of said evaluated elements (col. 7, lines 5-15 in Eaton teach that ECC Engine 3-3 of Figure 3 in Eaton is used to identify hard and soft errors at a memory location or cell; Note: a memory location or cell is a memory element and a means for determining a hard error is means for determining a faulty memory cell since hard errors are errors due to defective memory elements); determining a number of said identified faulty ones of said evaluated elements in each of a plurality of subsets of said memory segment (col. 5, lines 61-68 in Eaton teach that that each IC chip 3-1 in Figure 3 stores data records in subsets of the IC chip 3-1; col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a record; Note: a record is substantially a subset of a IC chip memory segment 3-1); comparing said determined number to a fault threshold value (col. 7, lines 17-21 in Eaton teaches that if the number of defects exceeds a criterion for acceptable

ECC engine 3-3 margin; Note: a criterion for acceptable ECC engine 3-3 margin is a threshold); declaring a failure condition for said memory segment if said determined number is greater than equal to said fault threshold value for any column of said memory segment (col. 7, lines 17-21 in Eaton teaches that if the number of defects exceeds, i.e., is greater than or equal to, a threshold for acceptable ECC engine 3-3 margin, then that group of defective memory cells is taken out of use, i.e., a failure for said memory segment is declared); and physically re-mapping said memory segment in response to said declared failure condition (col. 7, lines 21-24 in Eaton teaches that the group of declared defective memory cells are taken out of use and replaced or remapped to replacement memory cells 3-5c in Figure 3).

Col. 7, lines 5-15 in Eaton teach that ECC Engine 3-3 of Figure 3 in Eaton is used to identify hard and soft errors at a memory location or cell. A memory cell is a physical element on a semiconductor chip for storing data. One of ordinary skill in the art at the time the invention was made would have known hard errors are errors at a memory cell on a semiconductor chip at a physical location on the semiconductor chip. Col. 7, lines 21-24 in Eaton teaches that the group of declared defective memory cells are taken out of use and replaced or remapped to replacement memory cells 3-5c in Figure 3. The replacement memory cells are also physical elements having a physical location on a semiconductor chip. If a memory cell at a physical location on a semiconductor chip is found to be faulty, the faulty memory cell is remapped to a replacement memory cell at a physical location on the semiconductor chip that is presumed not to be defective. Figure

3 in Eaton explicitly depicts representations of physical memory cells. It would be nonsensical to allow the use of a known physically defective memory cell at a known physical site. The only thing that Eaton does not do is use the same language as the Applicant and it appears the Applicant is attempting to gain a patent on pure semantics and word games. However to accommodate the Applicant, the Examiner provides a new grounds of rejection whereby the same language that the Applicant uses is used in the Prior Arts for the grounds of rejection.

However Eaton does not explicitly teach the specific use of evaluating elements of said memory segment in row-fast order.

Harns, in an analogous art, teaches evaluating elements of said memory segment in row-fast order (col. 32, lines 12-15, Harns). Note: Eaton teaches testing and evaluating memory elements of a memory system but does not teach the details of how data is read out of memory during testing. Harns, on the other hand, teaches a commonly know means for reading data out of memory. One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine Eaton with Harns in order to provide a means for reading data out of memory in the Eaton patent. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Eaton with the teachings of Harns by including use of evaluating elements of said memory segment in row-fast order. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of evaluating

elements of said memory segment in row-fast order would have provided the means for reading data out of memory (col. 32, lines 12-15, Harns).

However Eaton and Harns do not explicitly use the language physically remapping.

Morley, in an analogous art, uses the language physically remapping (col. 4, lines 14-17 in Morley teach, "Upon detection of a "hard" error, the present invention can manipulate the appropriate address lines, including the chip-select lines and physically re-map the address space onto some spare semiconductor elements").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Eaton and Harns with the teachings of Morley by using the language physically remapping. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the language physically remapping would have provided would describe the operation of mapping defective memory cells at a physical location on a semiconductor chip as taught in Figure 3 of Eaton to non-defective replacement memory cells at a non-defective physical location on a semiconductor chip as taught in Figure 3 of Eaton (**Note also that since column and row address decoders are commonly implemented using counters successive scanning of rows is one of the most obvious and easiest way to implement a particular order for evaluating memory cells, reduced complexity is always a motivating factor and benefit**).

35 U.S.C. 103(a) rejection of claim 19.

The Examiner asserts that col. 5, lines 61-68 of Eaton teaches Reed-Solomon ECC check bits are used to check integrity of data after stored evaluation data is read out of an nxm memory cell array segment. One of ordinary skill in the art at the time the invention was made would have known that error checking for data d with check-bits c occurs by re-encoding data d to produce re-encoded expected check-bits c' whereby c' is compared to c to determine if an error has occurred (Note: comparing c to c' is equivalent to comparing stored d+c to expected data d+c', hence comparing c to c' is a step for comparing read stored evaluation data to expected data).

3. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton), Harns; Timothy (US 4460997 A) and Morley; Richard E. (US 4506362 A) in view of Bair; Owen S. et al. (US 6065134 A, hereafter referred to as Bair)

35 U.S.C. 103(a) rejection of claim 20.

Eaton, Harns and Morley substantially teaches the claimed invention described in claims 18 and 19 (as rejected above). The Examiner asserts that col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a subset. One of ordinary skill in the art at the time the invention was made would have known that a counter is a means for determining a number of defects in a subset. Note: the count only has to be retained for analysis of a record and afterwards must be reset to evaluate a new record in Eaton.

However Eaton, Harns and Morley do not explicitly teach the specific use of a failure counter.

Bair, in an analogous art, teaches that if a "memory cell is defective, row error counter Rec 43 increments 82 by one to maintain the correct count of the detected defective memory cells, and I/O error counter I/Oec 44 also increments 84 by one to track the correct count of the detected defective memory cells" (col. 5, lines 18-35 in Bair).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Eaton, Harns and Morley with the teachings of Bair by including use of a failure counter. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a failure counter would have provided the opportunity to implement the means for determining a number of defects in a subset taught in the Eaton patent (col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a subset).

4. Claims 21-25, 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) in view of Green; George D. et al. (US 4965799 A, hereafter referred to as Green).

35 U.S.C. 103(a) rejection of claim 21.

Eaton teaches determining a number of identified faulty ones of evaluated memory elements in each of a plurality of subsets of a memory segment (col. 5, lines 61-68 in

Eaton teach that that each IC chip 3-1 in Figure 3 stores data records in subsets of the IC chip 3-1; col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a record; Note: a record is substantially a subset of a IC chip memory segment 3-1); comparing said determined number to a fault threshold value (col. 7, lines 17-21 in Eaton teaches that if the number of defects exceeds a criterion for acceptable ECC engine 3-3 margin; Note: a criterion for acceptable ECC engine 3-3 margin is a threshold); declaring a failure condition for said memory segment if said determined number is greater than equal to said fault threshold value for any column of said memory segment (col. 7, lines 17-21 in Eaton teaches that if the number of defects exceeds, i.e., is greater than or equal to, a threshold for acceptable ECC engine 3-3 margin, then that group of defective memory cells is taken out of use, i.e., a failure for said memory segment is declared); and physically re-mapping said memory segment in response to said declared failure condition (col. 7, lines 21-24 in Eaton teaches that the group of declared defective memory cells are taken out of use and replaced or remapped to replacement memory cells 3-5c in Figure 3). Ina addition, Eaton explicitly teaches identifying faulty ones of said evaluated elements (col. 7, lines 5-15 in Eaton teach that ECC Engine 3-3 of Figure 3 in Eaton is used to identify hard and soft errors at a memory location or cell; Note: a memory location or cell is a memory element and a means for determining a hard error is means for determining a faulty memory cell since hard errors are errors due to defective memory elements). However Eaton does not explicitly teach the specific use of a specific **order** for evaluating defective memory cells, but leaves it open to any of the commonly known

techniques in the art for detecting defective memory cells such as successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements.

Green, in an analogous art, teaches a commonly-known **order** for evaluating defective memory cells by successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements (see steps l and m in claim 16 in col. 6 of Green; Note: a column is a linear array and a row is a second linear array which are subsets of a memory array typically fond in memory arrays forming a memory segment).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Eaton with the teachings of Green by including a commonly-known **order** for evaluating defective memory cells by successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that a commonly-known **order** for evaluating defective memory cells by successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements would have provided the required means in the Eaton patent for identifying faulty ones of said evaluated elements (col. 7, lines 5-15 in Eaton teach that ECC Engine 3-3 of Figure 3 in Eaton is used to identify hard and soft errors at a memory location or cell; Note: a memory location or cell is a memory element and a

means for determining a hard error is means for determining a faulty memory cell since hard errors are errors due to defective memory elements; **Note also that since column and row address decoders are commonly implemented using counters successive scanning is one of the most obvious and easiest way to implement a particular order for evaluating memory cells**).

35 U.S.C. 103(a) rejection of claim 22.

See steps l and m in claim 16 in col. 6 of Green.

35 U.S.C. 103(a) rejection of claim 23.

See steps n and o in claim 16 in col. 6 of Green.

35 U.S.C. 103(a) rejection of claim 24.

Col. 7, lines 17-21 in Eaton teaches that if the number of defects exceeds, i.e., is greater than or equal to, a threshold for acceptable ECC engine 3-3 margin, then that group of defective memory cells is taken out of use, i.e., a failure for said memory segment is declared. Col. 8, lines 56-58 in Eaton teaches that a flag is used to indicate an uncorrectable error, i.e., when the number of defects exceeds the threshold for acceptable ECC engine operation.

35 U.S.C. 103(a) rejection of claim 25.

There is no indication that any of the results of the Reed-Solomon such ad CRC differences or syndromes are saved and are most likely discarded when the error correction engine is done as is generally done in Reed-Solomon decoding.

35 U.S.C. 103(a) rejection of claim 27.

The Examiner asserts that col. 5, lines 61-68 of Eaton teaches Reed-Solomon ECC check bits are used to check integrity of data after stored evaluation data is read out of an nxm memory cell array segment. One of ordinary skill in the art at the time the invention was made would have known that error checking for data d with check-bits c occurs by re-encoding data d to produce re-encoded expected check-bits c' whereby c' is compared to c to determine if an error has occurred (Note: comparing c to c' is equivalent to comparing stored d+c to expected data d+c', hence comparing c to c' is a step for comparing read stored evaluation data to expected data).

35 U.S.C. 103(a) rejection of claim 28.

Defective cells are a characteristic of an nxm memory cell array segment.

5. Claims 26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) and Green; George D. et al. (US 4965799 A, hereafter referred to as Green) in view of Bair; Owen S. et al. (US 6065134 A, hereafter referred to as Bair)

35 U.S.C. 103(a) rejection of claim 26.

Eaton and Green substantially teaches the claimed invention described in claims 26 (as rejected above). In addition, there is no indication that a total number of defects are kept for any subset in the Eaton patent for longer than what they are needed. Only the number of defects in a subset are determined.

However Eaton and Green do not explicitly teach the specific use of avoiding recording a total number of said counted malfunctioning elements in said memory segment.

Bair, in an analogous art, teaches avoiding recording a total number of said counted malfunctioning elements in said memory segment. Bair, in an analogous art, teaches that if a "memory cell is defective, row error counter Rec 43 increments 82 by one to maintain the correct count of the detected defective memory cells, and I/O error counter I/Oec 44 also increments 84 by one to track the correct count of the detected defective memory cells" (col. 5, lines 18-35 in Bair). A counter is a means for avoiding recording a total number of said counted malfunctioning elements in said memory segment.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Eaton and Green with the teachings of Bair by including use of a failure counter for avoiding recording a total number of said counted malfunctioning elements in said memory segment. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a failure counter for avoiding recording a total number of said counted malfunctioning elements in said memory segment would have provided the opportunity to implement the means for

determining a number of defects in a subset taught in the Eaton patent (col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a subset).

35 U.S.C. 103(a) rejection of claim 29.

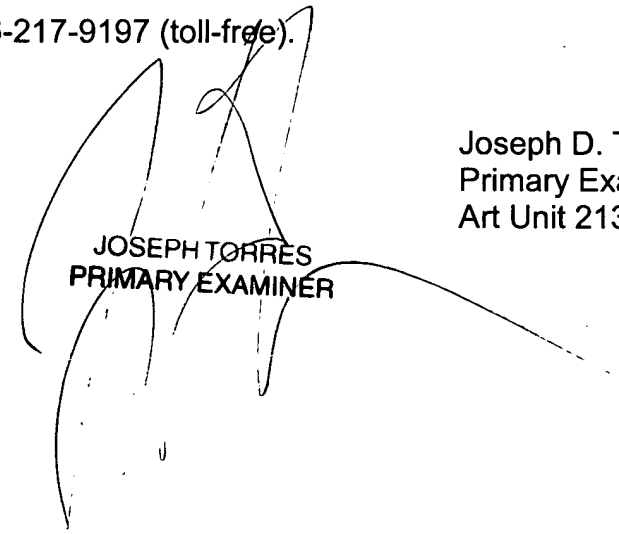
See Step 43 in Figure 2 of Bair.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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